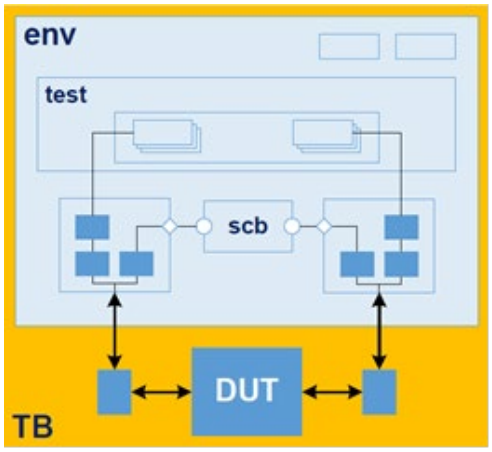
fidus
innovate•design•deliver

high speed, high complexity

VERIFICATION (UVM)



How we help

Want to: Improve your **design quality**? Lower your **risk**? Achieve "**first time right**"? Create a **re-usable** Verification environment? Stay **focused** on your core competency?

Fidus has extensive experience in Digital Design Verification through the planning and implementation of re-usable verification environments, and supports UVM™, SystemVerilog, and SystemC® software. We preserve your investment in legacy simulation environments/tools, help you transition to newer methodologies, and build new verification environments to achieve your quality goals.

Fidus – an excellent choice

At Fidus Systems, we understand the unique challenges faced by technology companies – too many projects and too few engineering resources. With top engineering talent, multiple design centers and on-site staffing options, Fidus provides highly responsive engineering teams that are an extension of your development team to successfully bring products to market faster.

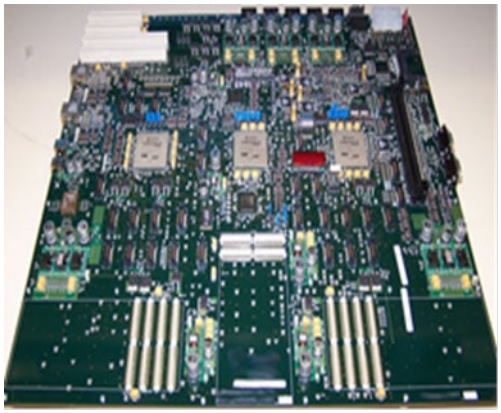
Recognized as a trusted design partner, Fidus is dedicated to meeting customer expectations, and developing long-term relationships with clients built on integrity, quality and open communications.

Fidus is pleased to provide customers with full end-to-end development solutions or more selective targeted engagements.

Fidus has delivered more than 1500 projects for 300+ clients, from Tier-1 multinationals to SMEs to start-ups. Fidus is headquartered in Ottawa, Canada with local design centers in Kitchener-Waterloo and Silicon Valley

Verification Expertise

- **Expertise:** We do full FPGA and ASIC/SoC verification, using UVM, SystemVerilog, and SystemC
- **Engagement Models:** We offer flexible engagement models, ranging from consulting to full turnkey verification environments
- **Test bench migration:** We can migrate your directed test benches to methodology based, reusable, coverage driven, constrained random testbench environments with live tracking capabilities
- **Team Bring Up:** We offer planning and configuration set-up that will train your development and management teams on the benefits, savings, and de-risking techniques leveraged in Verification
- **Verification Planning:** In scenarios where we bring specific domain expertise, we can provide the entire planning process. When the domain expertise resides with you, we provide consulting to coordinate your planning effort. In addition, we help you reach your quality goals through feature categorizing and live test-plan creation.
- **Verification IP:** We source verification IPs for standard protocols like AMBA, AXI, PCIe, SRIO PCIe Bridging, NVMe, WiFi 802.11 variant PHY and MACs, Ethernet, DDR, USB, SATA, AHCI, SerDes, UART, I2C, DDR, HDLC controllers, etc.
- **Constrained Random Verification (CRV):** We offer constrained random verification services to augment your existing environments
- **Assertion-Based Verification (ABV):** We can train your design and verification teams on Assertion-Based Verification and will bind, track and measure these in your existing environments
- **Directed Testing:** For simple FPGA flows, we can offer Directed Testing solutions



XILINX® | ALLIANCE PROGRAM PREMIER MEMBER

Bringing you Xilinx premier

As Xilinx Premier, Fidus receives exclusive training, certification, and early-access to tools, IP, and new silicon. By invitation, Fidus was ***the*** inaugural Xilinx Premier Design Services member in North America. So what does this mean? It means that when you hire Fidus, you know that Fidus is on the forefront of Xilinx's roadmap, experienced in the most advanced tool flows, and is top of mind within the Xilinx support network.

Examples of our work

FPGA Verification

- Numerous FPGA vendors/families (e.g. Xilinx®, Intel®/Altera™)
- Diverse set of systems and protocols, including DSP
- Full range from Directed Testing for simpler FPGAs to Constrained Random/UVM Verification for complex FPGAs

ASIC Verification

- Wireless signal processors/60G Wireless Modems
- High Performance Virtualized Network Interface Controllers
- High-end Server Processors
- DDR Clock Drivers and Buffers
- PCIe Bridges
- Mixed analog/digital designs with

Tasks undertaken

- Translate design specs into verification requirements
- Architect block/top level verification environments
- Develop verification plans, schedule estimation, and tracking
- Enhance pre-existing verification environments with UVM verification methodologies
- Design and implement verification components; reference models, scoreboards, agents, etc.
- Integrate bit accurate reference models from MATLAB into functional SystemVerilog test-benches (e.g. DSP)
- Incorporate and configure external Verification IP
- Implement coverage models, collect coverage data, and achieve coverage closure
- Manage simulation regressions, triage and fix regression failures
- Adopt and support continuous integration techniques related to hardware development
- Investigate, evaluate, and recommend new tools in the spirit of continuous improvement
- Create scripts for improved verification productivity
- Collaborate with rapid prototyping, test, validation, and software teams

The Team Approach

Fidus' Verification experts de-risk your Program while creating an environment that will be used to de-risk your future Programs. For end-to-end design and verification, Fidus also offers FPGA, Hardware, Software, and Signal Integrity design experts to support your project.

About Fidus

Fidus Systems, founded in 2001, specializes in leading-edge electronic product development with offices in Ottawa and Waterloo Ontario, and San Jose, California. Our hardware, software, FPGA and signal integrity teams architect, design and deliver next-generation products for clients in emerging technology markets. We build long-term relationships by consistently exceeding expectations.

Ottawa • Waterloo • Silicon Valley