

## Product Outline

Ideal for defense, video, and comms developments

### Featuring

- Xilinx® Kintex® UltraScale™ XCKU115-2FFVA1517
- Xilinx® Zynq® XC7Z010-2CLG225I

### FPGA Subsystem

- Four (4) FMC interfaces (see table)
- 16.375Gbps transceivers (see table)
- Memory
  - 4 GB DDR4 SDRAM on board
  - 2 controllers, 64-bit bus-width
  - Maximum theoretical throughput: 215 Gbps
- Clocking, onboard
  - Si5338 programmable clock generator
  - Si5347 quad PLL (jitter filter and re-transmission)
  - 156.25MHz SFP+ oscillator
  - 200MHz DDR4 clock
  - SMA's, including, CLKin, CLKout, SyncIn, SyncOut
- SFP+ interface
- UART-over-USB support
- Miscellaneous, general purpose
  - 8 DIP Switches, 4 push-button switches
  - 8 User Selectable Header Inputs
  - 8 LEDs (4 red, 4 green)
- JTAG over USB, JTAG header, Dual Quad SPI Flash

### Zynq ARM®-based Subsystem

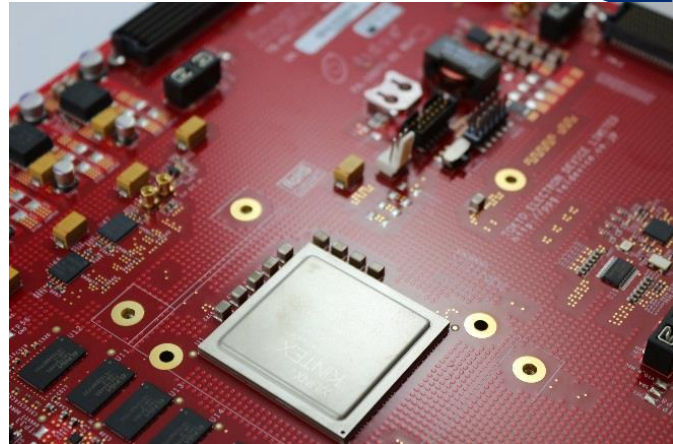
- CLI, Micro USB (UART-over-USB)
- JTAG, DAP 14-pin header
- uSD interface
- 8 general purpose LEDs (3 red, 5 green)
- 4 general purpose DIP switches

### Power

- External 12VDC power supply (included)

### Board Dimensions

- 280mm x 200mm (approx. 11" x 8")



## Features

- Kintex UltraScale XCKU115-2FFVA1517
- Four (4) FMC Interfaces
- 4 GB DDR4 SDRAM
- Flexible clocking architecture, featuring
  - Multiple clocks
  - Programmable clock generator, Quad PLL
- Onboard Zynq for system management and processing
- SFP+ interface
- General purpose LEDs and switches
- Proven operation with inrevium HDMI4K, 12G-SDI, DP1.2, V-by-One®, MIPI, and Zynq FMCs
- Compatible with FMC Specification (VITA 57.1)

## FMC Slot Capabilities

	IO ASSIGNMENTS			
	GTH	LA	HA	VADJ (V)
FMC0	DP[9:0]_M2C DP[9:0]_C2M	LA[33:0]	HA[4:0]	1.8,2.5,3.3
FMC1	DP[9:0]_M2C <sup>1</sup> DP[9:0]_C2M <sup>3</sup>	LA[33:0]	N/A	1.5, 1.8 (common VADJ)
FMC2	DP[9:0]_M2C DP[9:0]_C2M	LA[18:0] LA[23:19] <sup>2</sup>	N/A	
FMC3	DP[9:0]_M2C DP[9:0]_C2M	LA[33:0]	N/A	

<sup>1</sup> Verify your target FMC with us prior to ordering

<sup>2</sup> Single ended support only

<sup>3</sup> Due to the SLR split, 10 GTHs are available but only 8 can be grouped

## Available References

### Included IP

- DDR4 Memory Controller
- Chip2Chip Interface Block

### Design Package (available under license)

• Schematics, PCB Layout, Artwork, Bill of Materials

### FPGA Reference Designs

- Downloadable .bit file examples
- Licensable source (some blocks netlist encrypted)

## Sales - Ordering Enquiries

For additional information, questions or request for quotation visit: [www.fidus.com](http://www.fidus.com)

## Customize your TB-KU-115-QUATTRO

Speak with our Design Services Group on how to accelerate your custom design: [design@fidus.com](mailto:design@fidus.com)

## About Fidus

Fidus Systems, founded in 2001, specializes in leading-edge electronic product development with offices in Ottawa and Waterloo Ontario, and San Jose, California. Our hardware, software, FPGA and signal integrity teams architect, design and deliver next-generation products for clients in emerging technology markets. We build long-term relationships by consistently exceeding expectations.

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**Figure 1: Block Diagram**

