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PRODUCT BRIEF

mantyss™ 32G

The Solution for Prototyping High-Speed Interfaces and Arm® SoCs on HAPS

Overview

The Synopsys HAPS-70 and HAPS-80 Prototyping Systems provide a fast and reliable way to prototype new ASIC and SoC designs and have been designed to deliver easy integration with physical interfaces in as short a time as possible.

Prototyping the physical interfaces inherent in the HAPS systems is straight forward and is core to the systems functionality. However, designers can face challenges when the interfaces they are integrating into their ASIC are not readily available, or if these interfaces are available as external components that are not seamlessly integrated into the platform. To resolve this, the HAPS System provides HapsTrak 3 (HT3) connectors that allow custom daughter cards to be directly connected and integrated into the HAPS system.

A major challenge in the HAPS ecosystem is the lack of interfaces that enable prototyping in the context of real-world speeds. In addition, modern SoCs integrate multiple Arm cores that require native prototyping.

There are two interfaces that are used by the newest versions of ASICs/SoCs that would benefit from tighter integration into the HAPS system:

- High-speed serial interfaces, like those that are combined to assemble 100GigE, 400GigE, PCIe Gen4/Gen5 protocols, or other interfaces requiring multi-gigabit SerDes
- Designs using integrated Arm processors

This whitepaper explores options for prototyping these new interfaces in the HAPS system, and how the flexibility of using technology-specific daughter cards connected to the HAPS system through the HapsTrak 3 (HT3) connectors increases the capabilities of the system.

Background

As bandwidth demands continue to increase within and across markets and applications, the demand for underlying high-speed transceivers will continue to increase. In addition, the complexity and implementation risk will increase as switching frequencies are pushed. For instance, PCIe Gen4, which requires 16Gbps per channel, is currently in the market and device manufacturers are adding it to an increasing number of their ASICs. PCIe Gen5 is on the horizon with the need for 32Gbps serial links and will further increase the need for ASIC designers to provide this capability within their devices. As protocols like 100 and 400 Gigabit Ethernet become more mainstream, as 5G gains traction, and as high-performance computing demands faster interfaces into memory and processing, the need for the ASIC and custom SoC manufacturers to respond to these high-speed interfaces increases.

In addition to higher speed physical interfaces, there is a trend toward increasing the capabilities of the ASIC by integrating processor cores, like Arm, onto the die. These SoCs provide the customer greater integration and flexibility when implementing a product design. By integrating these SoCs onto a HAPS systems, designers can accelerate their software development and verification of Arm-based systems.

Prototyping these chip designs using the HAPS system is an important step before going to tape-out. When verifying high speed interfaces, existing solutions do not reach the 32Gbps speeds, are as integrated, or provide the flexibility of the MPSoC (Zynq® UltraScale+™) directly available to the HAPS system. For Arm processor designs, previous methods required the integration of several different components through external cabling and did not provide the benefits of the tighter integration with HAPS.

To address the limitations of the HAPS systems, an integrated HAPS daugher board that combines Arm processors and high-speed transceivers was developed.

This whitepaper describes the use of the Mantyss-32G HAPS Daughter Card, including the flexibility of having access to its Xilinx® Zynq® UltraScale+™ FPGA to support the prototyping of 32Gbps SerDes links used in current and next generation communications protocols. By allowing the designer complete access to both the quad-core Arm Processor Subsystem (PS) and the large transceiver-enabled Programming Logic (PL) to prototype their devices, designs can be quickly set up and prototyped using HAPS.

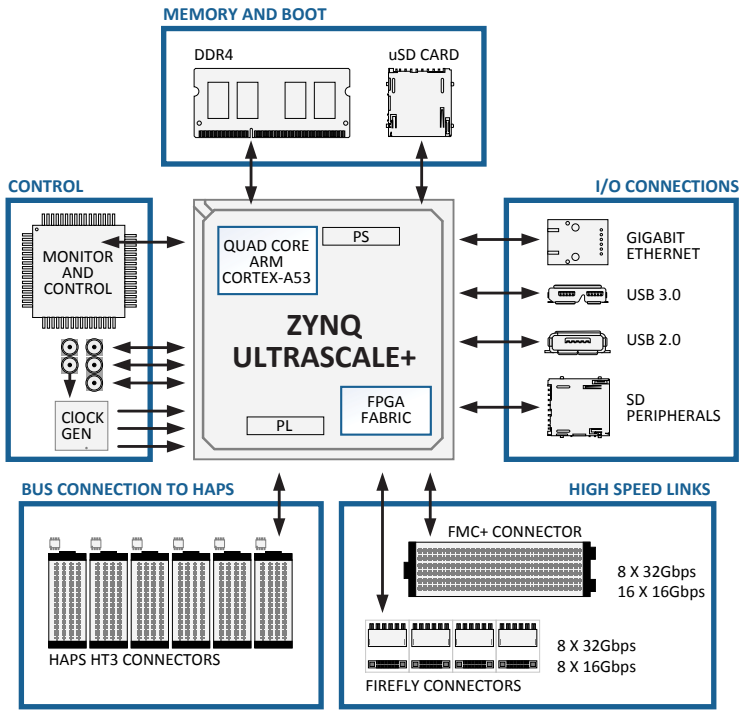
The Mantyss-32G™ HAPS daughter card enables an integrated solution, improves efficiency in setup and implementation, and expands the capacity and capabilities of the HAPS Prototyping Solution.

High-speed SerDes and Arm Prototyping Integration into HAPS

When external I/O peripherals are required on HAPS, there are several ways of getting the data into the HAPS system. These typically involve an external circuit card that is powered and programmed separately, cabling into the HAPS system, and a HAPS configuration to recognize the external peripheral. The complexity, configuration, and cabling of this system can lead to longer setup and debug times, which often results in lower overall system performance.

An integrated daughter card has several advantages in combining external peripherals:

1. The physical connection to the HAPS system is made through the HT3 connections. This is physically more compact and reliable, provides a tighter level of integration with HAPS for higher-speed data transfer and signaling, and allows for greater flexibility in configuration and prototyping options.
2. The power needed for the daughter card can use the same PSU used by the HAPS prototyping system.
3. The ProtoCompiler integration allows HAPS to fully understand and take advantage of the new functionality available to it on the daughter card.
4. IP that requires the daughter card's additional functionality can be created and can rely on a consistent interface to the daughter card and its functionality.
   - IP is already available that takes advantage of this - PCIe Gen4 is one example
5. Since the daughter card and its connections have been verified by Synopsys to operate at full speed with the HAPS system, faster bring-up times are possible as the level of debug typically required to enable externally cabled cards is greatly reduced.



Mantyss-32G Architecture

Additional flexibility is provided when the daughter card contains an MPSoC, with its internal Arm cores PS and FPGA fabric that is made completely accessible to the user.

Using a daughter card with an MPSoC gives the user the opportunity to expand their application to take advantage of this additional infrastructure.

The Mantyss-32G HAPS Daughter Card, centered around a Xilinx Zynq UltraScale+ MPSoC, significantly increases the I/O speed and prototyping capabilities of the HAPS system, and provides the benefits needed by users wishing to expand their HAPS prototyping capabilities.

This MPSoC provides the following features which are fully accessible from the HAPS system:

- **Capability:** Fully accessible XCZU19EG-3 Zynq UltraScale+ MPSoC with direct access to the HT3 connectors that tightly bind it into the HAPS system
- **Speed:** Highest speed grade (-3) available for this part, with verified operation to 32Gbps on 16 lanes (GTY) and an additional 16Gbps on 24 lanes (GTH). This increases the standard HAPS support of 10Gbps across 10 transceivers to 32Gbps/16Gbps across 40 transceivers
- **Fabric:** 1,143k System Logic Cells in the PL, the largest in this series. This PL is in addition to the PL provided in HAPS
- **ARM Processors:** Quad core Arm Cortex®-A53 processor with dual core Cortex-R5 real-time processors and a Mali-400 MP2 GPU in the PS, with complete Arm trace capability. Can be used to prototype an Arm design, be used to manage data flow, or for monitoring/control
- **Data Movement:** 12 x 32/64/128b AXI Ports as the PS to PL Interface
- **Expansion:** VITA 57.4 Compatible FMC+ connector to expand the I/O that is accessible to HAPS by connecting FMC cards onto the Mantyss Daughter Card. This could include FMC cards that handle video, QSFP communications, mixed signal, or any other speciality interfaces
- **External Connections:** Board-to-board FireFly™ connections (both optical and copper) to consolidate external components into HAPS or to support flexibility in getting data into the HAPS prototyping system
- **Clocking:** Fully configurable clocking subsystem with multi-clock generators, jitter attenuators, and MMCX clock inputs and outputs to provide the correct clocking for your applications
- **Interfaces:** Standard interfaces such as USB3.0, GigE, JTAG ports, along with on-board 16GB x72 DDR4 memory
- **Management:** Board controller that manages configuration, control, power monitoring, and thermal monitoring

A Mantyss-32G Daughter Card mounted on a HAPS-80 Prototyping Solution

Technology examples

PCIe Gen4/5 Prototyping

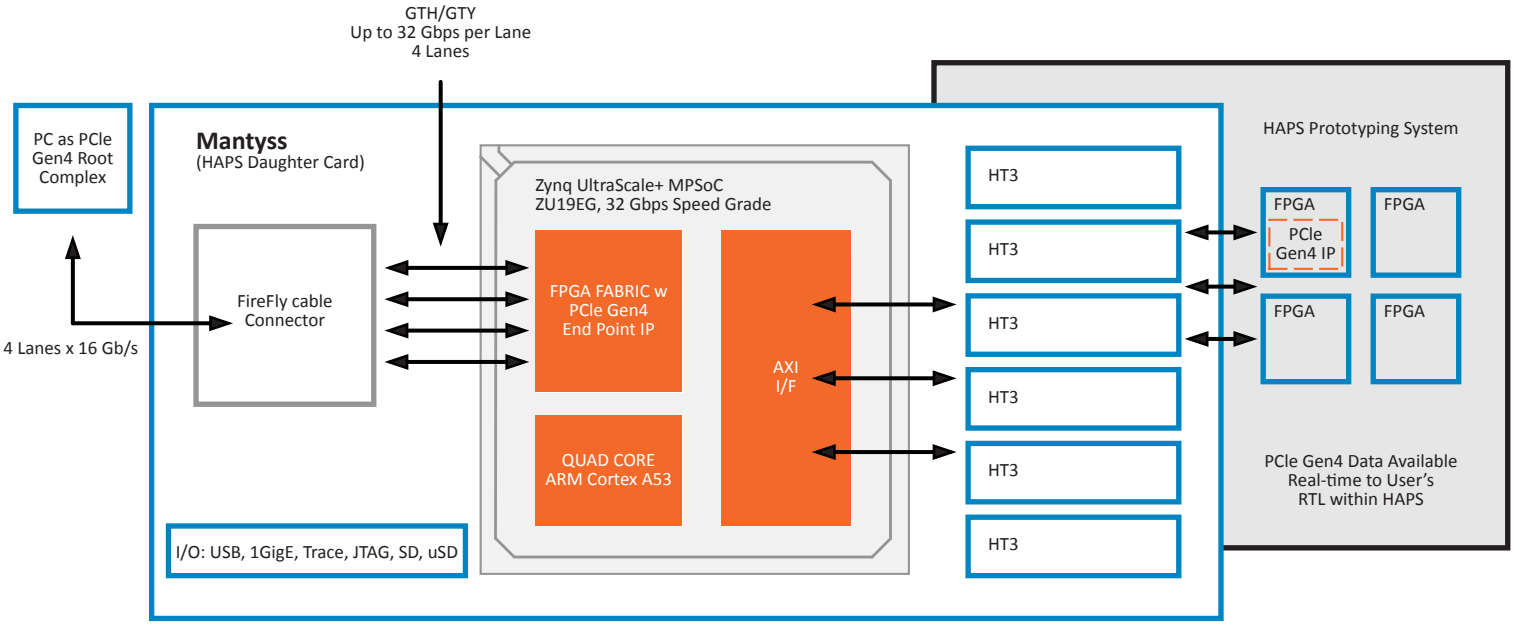


Figure 1:
Data Flow into HAPS for a PCIe Gen4 End-Point Example, using the Mantyss Daughter Card

As PCIe Gen4 is adopted in current IC designs, and as PCIe Gen5 emerges, there is increasing demand to prototype these solutions. Synopsys currently offers PCIe Gen 4 IP that is compatible with the Mantyss Daughter Card.

While there are various options about how PCIe data is brought into the system, **Figure 1** is an example where a PC acts as the PCI Root Complex, and transfers data to the Mantyss Daughter Card through a Samtec FireFly connector, and into the Zynq US+ MPSoC. Synopsys supplied IP on the Daughter Card, transfers the data into HAPS through the HT3 connectors, and is made available to the designer's DUT RTL that has been set up by ProtoCompiler.

To prototype PCIe Gen5 applications, designers may consider creating IP that would reside on the Mantyss HAPS Daughter Card directly since the Zynq US+ MPSoC has a large, fully accessible fabric and configurable clocking.

100 / 400 Gig Ethernet Prototyping

100 GigE and 400 GigE are also technologies that designers are being asked to prototype. **Figure 2** shows a data flow for a 100 GigE design that brings data into the HAPS system through the Mantyss Daughter Card.

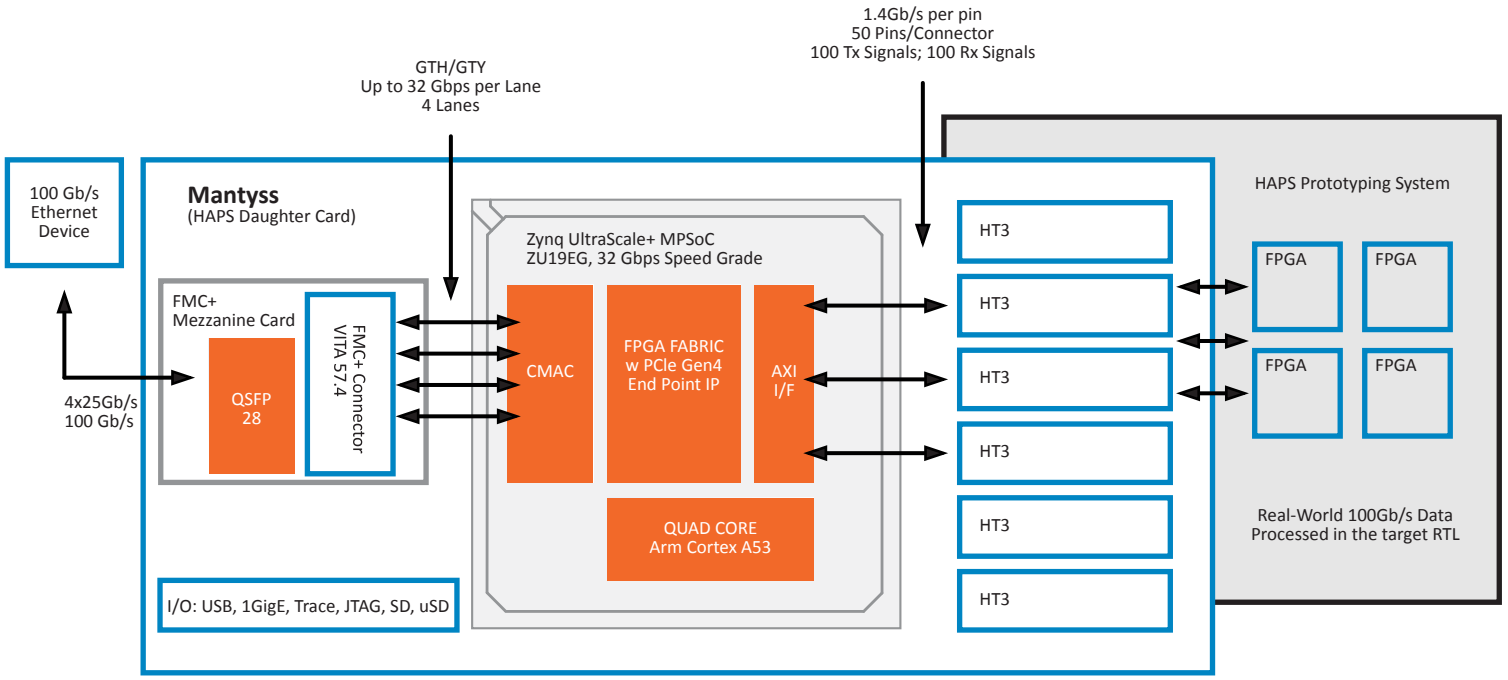


Figure 2:
Data Flow into HAPS for 400/100 Gig Ethernet, using the Mantyss Daughter Card (100Gb/s shown)

In this architecture, four lanes of 25.78125 Gbps are brought onto the Mantyss Daughter Card through a QSFP28 FMC card attached to Mantyss (these are readily available). Data flows into the Zynq MPSoC, where the hardened CMAC manages the MAC functionality, and provides the data to the rest of the system using AXI over the HT3 connectors.

There are many possibilities of pre-processing, in-line packet inspection, monitoring, capturing, or peek/poke using the Zynq MPSoC on the Mantyss Daughter Card, since the user has access to the entire PL and PS within the device that will allow them to manipulate the incoming or outgoing bitstream if they choose.

Moving the CMAC

Figure 3 demonstrates some of the system's flexibility and ways the architecture can be modified depending on the code that the designer wants to verify.

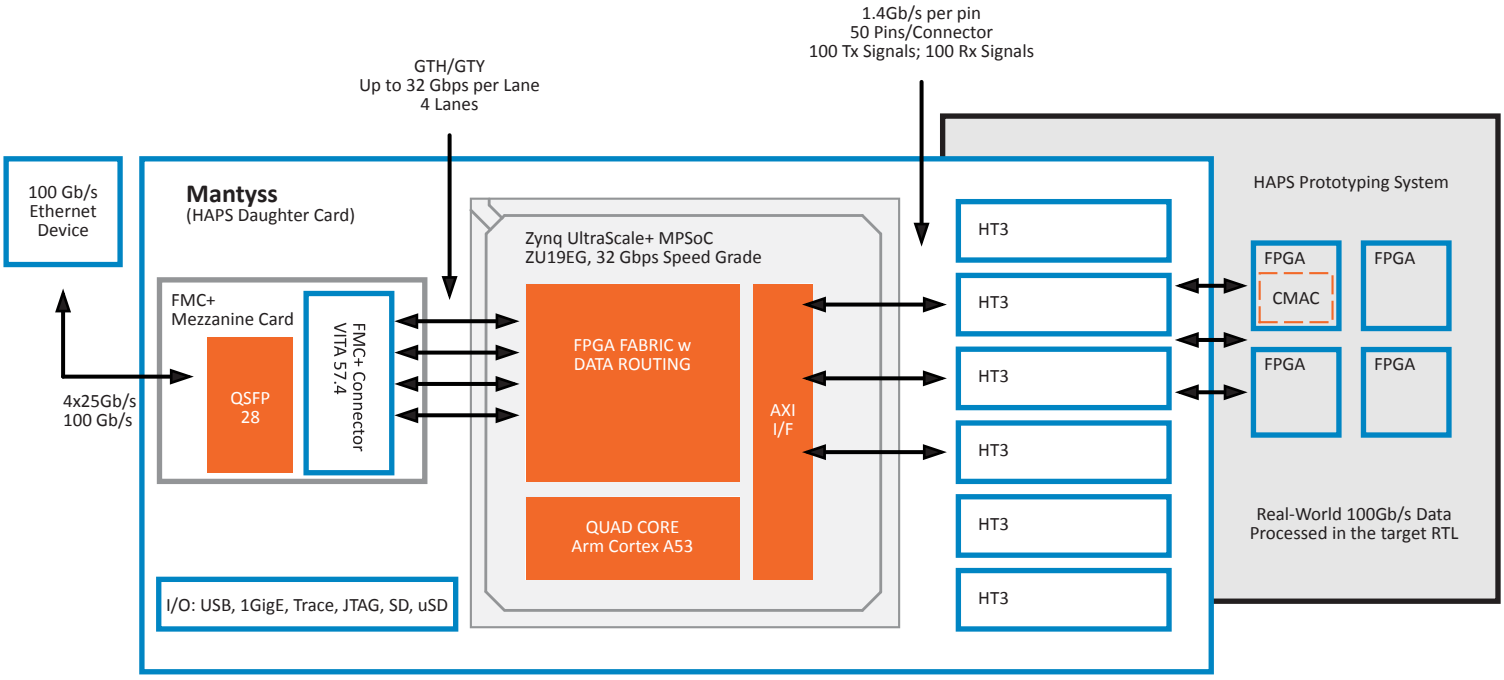


Figure 3:
100 Gigabit Ethernet Data Flow with CMAC located in HAPS Prototyping System

In the case where the PHY and ethernet stack are the target of the verification, these items can be either instantiated on the Zynq FPGA on the Mantyss Daughter Card and run there, or they can be moved into the HAPS prototyping system using ProtoCompiler. In the latter case, the Zynq FPGA located on the Mantyss Daughter Card would route the raw ethernet packets over the HT3 connectors into the HAPS system in real time.

Arm Prototyping

The quad-core Arm processor available on the Mantyss Daughter Card allows users to prototype Arm-based SoC designs in a much more integrated way.

Previous whitepapers have been written about using the JUNO development platform to prototype a design on HAPS. While this solution did meet the need at the time, it consists of an external board that is cabled over the HAPS in a non-integrated way. The Mantyss Daughter Card connects directly to the HAPS system and is visible within ProtoCompiler in a way that was not available previously, offering a much better alternative for prototyping Arm designs on HAPS. The Arm cores on the Zynq SoC on Mantyss are 100% available to the user and include TRACE debug capability via a dedicated Arm-JTAG connector interface.

As the need for Arm processors within IC designs increases, this simpler and more integrated approach improves prototyping efficiency, and provides a high-bandwidth link between the Arm sub-system and the programmable logic region.

New or Alternate Applications - Arm Transaction Tracking

High speed Arm transaction tracking is a way of demonstrating non-traditional applications and the flexibility of the HAPS / Mantyss Daughter Card platform. **Figure 4** shows a solution where transactions are monitored within the test environment and either buffered or live streamed to and from a server running Arm tracking software. Arm has specifically designed this server software to enhance their tracking and trace capabilities to get greater insight into the AMBA bus.

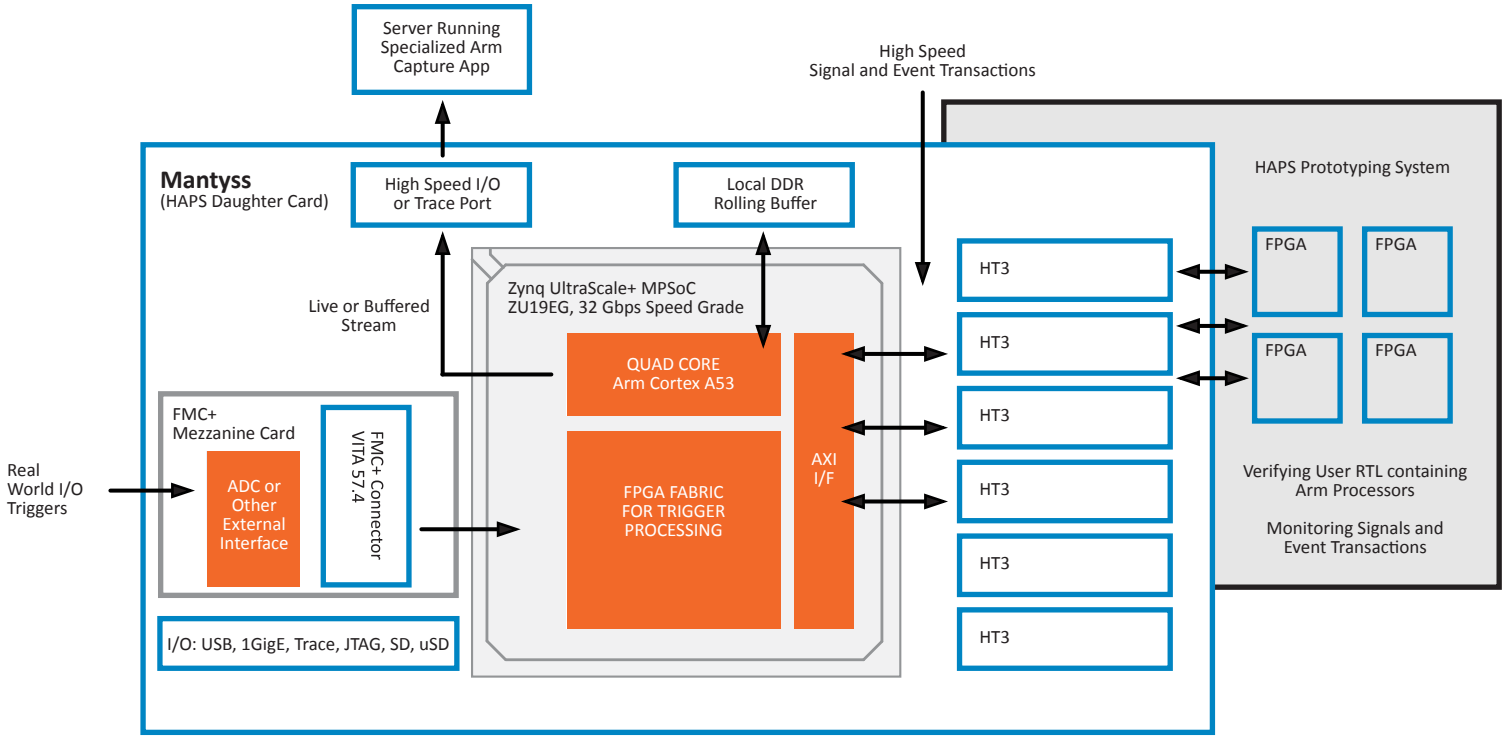


Figure 4:
ARM Transaction Tracking using the Mantyss Daughter Card

Transactions are monitored and data streamed to the Zynq FPGA on the Mantyss Daughter Card, where it is either live streamed or stored locally waiting for a trigger. Data is then transferred to a Server running trace software that allows the user to monitor and debug their Arm instantiation. This example shows external I/O triggers brought in through the FMC card and processed within the MPSoC fabric, but that trigger can be external, internal, or logically derived.

The HAPS and Mantyss Daughter Card together provide increased options to users wanting to prototype their designs. Other technologies not mentioned in this paper, an SDR Mixed signal ASIC, for example, could benefit from the ability to bring in varying I/O interfaces and the flexibility of having access to the Zynq MPSoC platform.

Conclusion

The demand for higher speed interfaces and more integrated prototyping environments is being driven by the new, higher performing protocols and technologies. The higher speeds, costs, and schedules of IC design and tapeout, means that IC Manufacturers, now more than ever, need to fully verify their designs. As such the prototyping tools and IP must keep pace with these new demands. The HAPS Prototyping Solution is a way to reduce the time to prototype and its capabilities have been further enhanced by the Mantyss Daughter Card for HAPS.

The Mantyss Daughter Card provides the high-speed interfaces needed to address these new technologies by creating a flexible front end using an FMC+ or FireFly interface, by providing a Zynq ZU19EG MPSoC fully accessible to the designer so that they can pre-process incoming data, use its fabric and Arm cores to monitor and control data flow, or to instantiate portions of the RTL design being verified to offload portions of it from the HAPS system.

In addition to the high-speed requirements, more devices are now integrating Arm processors into their IC designs. Prototyping these processors used to mean that external cards had to be cabled into the HAPS system. With the on-board quad core Arm processors and access through TRACE available for prototyping on the Mantyss Daughter Card, this solution is now much more integrated into the HAPS system.

This whitepaper demonstrated a few architectures that address the prototyping needs of the next generation technologies being designed into new ICs. Given the I/O and processing flexibility that the Mantyss Daughter Card provides to HAPS, the system is designed to be adaptable to handle many other current and future technologies.

Enable your high-speed prototyping with the Fidus Mantyss-32G.

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For additional information, questions or request for quotation visit: **mantyss.fidus.com**

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Mantyss Ecosystem

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