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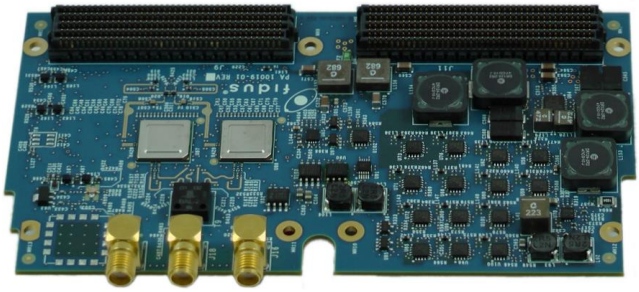
Single Channel, 5GSPS, JESD204B ADC FMC

Part Number : FSF-AD15000A

5GSPS (equivalent) 12-bit, JESD204B ADC FMC



The FSF-AD15000A is a single channel analog-to-digital conversion board based on two Analog Devices AD9625 single-channel, 12-bit, 2.5 GSPS ADCs.

Product Outline

The FSF-AD15000A is a single input analog-to-digital converter FMC, designed to be electrically and mechanically compatible with the ANSI/VITA 57.1 specification. Using two AD9625 ADCs clocked on opposite edges of a low jitter 2.5 GHz clock, a 5 GSPS interleaved data stream is produced.

The interleaving process results in unwanted spectral content due to imbalances that exist in all interleaved sampling systems (e.g. gain, phase, DC offset - both within and external to the ADCs). All of these factors have to be digitally reduced or cancelled, for the final 5GSPS stream to be of full value. Fidus can provide the interleaving compensation IP in addition to the hardware. This IP is fully functional in the demo .bit file, but ultimately times out.

Features

- Single input, 12-bit, 5 GSPS (equivalent) ADC in a double-width HPC FMC form-factor
- JESD204B Subclass 1 feature set including deterministic latency
- Designed for compatibility with ANSI/VITA 57.1
- Analog input bandwidth: 0.5 MHz – 3.3 GHz
- Extremely low phase noise onboard oscillator, with analog clock distribution topology for source phase-noise preservation
- External clock and trigger inputs
- Designed for experimentation, development, and integration into end systems
- 0 to +45˚C operating temperature range*
- Xilinx® VC707 .bit file demonstration design
- Designed for compatibility with Xilinx® VC707 and VC709. Reference design available for VC707.
- ADC Multiple Device Synchronization (MDS) for coherent sampling across all ADC channels (JESD204B class MCDA-ML)
- Powered entirely through the FMC connector

*** Components are rated from -40 to +85˚C. Boards are only tested and characterized from 0 to 45˚C.**

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Interleaving is also attainable because of the deterministic latency feature of JESD204B. Without deterministic latency, one would not be able to guarantee the desired 180° timing offset of the samples from each ADC. This feature ensures that across resets and power cycles, each interleaved sample is phased correctly.

JESD204B also offers benefits at the physical layer. Once sampled, the data from each ADC channel is transmitted on a high-speed serial bus to the downstream device. This serial data architecture minimizes downstream I/O pin count and increases performance by lowering system noise. Similarly, PCB layer count requirements are relaxed compared to a parallel or multi-lane LVDS data bus design. Essentially, the serial nature of JESD204B makes this design practical. The FSF-AD15000A requires a total of 16 multi-gigabit transceiver lanes (8 lanes per link), with each lane running at 6.25 Gbps, driving the need for a double width FMC.

Extra care has been incorporated in the design of the FSF-AD15000A to ensure extremely low jitter on the ADC sampling clocks. Low jitter performance is critical in preserving the full dynamic range of the converters when high frequency analog inputs are exposed to both wanted and unwanted wide dynamic range signals.

The FSF-AD15000A is an ideal starting point for broadband, high fidelity waveform digitization experimentation. It is also a great platform to get up and running quickly with a JESD204B interface. Finally, it serves equally well as a ready-made drop-in solution for end-systems that require high sample rate, high fidelity, waveform digitization.

Applications

General experimentation and instrumentation
Test and measurement (e.g. mass spectrometry)
Wideband Radar
Signals Intelligence (SIGINT)

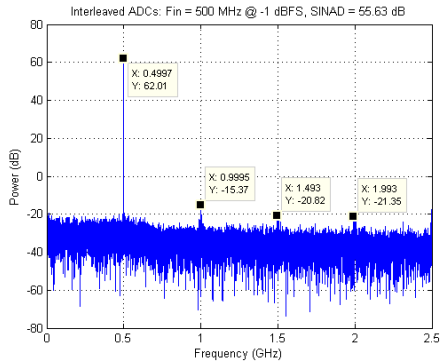
Typical Performance Characteristics

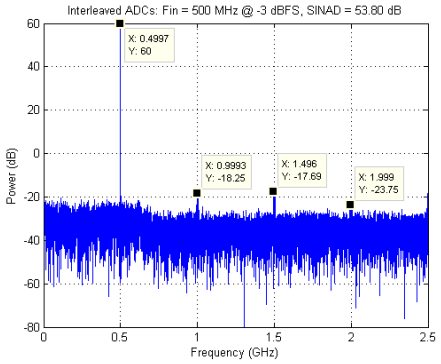
Test conditions

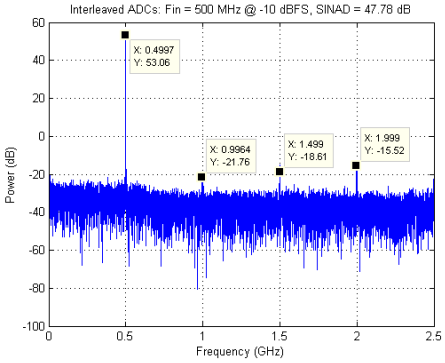
Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Enabled, Forced Convection (bench top fan), Limited sample size to date

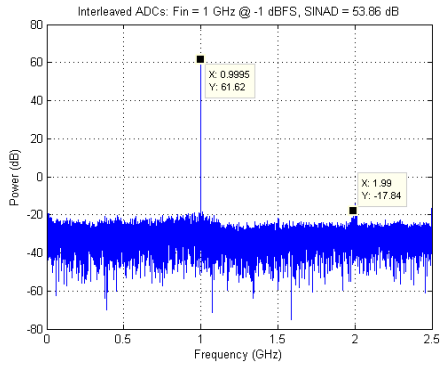
Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
ANALOG INPUT	Full scale	25°C		+18		dBm
ANALOG INPUT BW	-3 dB	25°C		3.3		GHz
SIGNAL-TO-NOISE RATIO (SNR)						
500 MHz	-1 dBFS	25°C		55.7		dBc
500 MHz	-3 dBFS	25°C		53.8		dBc
500 MHz	-10 dBFS	25°C		47.8		dBc
1000 MHz	-1 dBFS	25°C		53.9		dBc
1000 MHz	-3 dBFS	25°C		52.4		dBc
1000 MHz	-10 dBFS	25°C		46.7		dBc
SIGNAL-TO-NOISE AND DISTORTION (SINAD)						
500 MHz	-1 dBFS	25°C		55.6		dB
500 MHz	-3 dBFS	25°C		53.8		dB
500 MHz	-10 dBFS	25°C		47.8		dB
1000 MHz	-1 dBFS	25°C		53.6		dB
1000 MHz	-3 dBFS	25°C		52.4		dB
1000 MHz	-10 dBFS	25°C		46.7		dB
EFFECTIVE NUMBER OF BITS (ENOB)						
500 MHz	-1 dBFS	25°C		8.95		Bits
500 MHz	-3 dBFS	25°C		8.64		Bits
500 MHz	-10 dBFS	25°C		7.64		Bits
1000 MHz	-1 dBFS	25°C		8.65		Bits
1000 MHz	-3 dBFS	25°C		8.42		Bits
1000 MHz	-10 dBFS	25°C		7.46		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR)						
500 MHz	-1 dBFS	25°C		75.2		dBc
500 MHz	-3 dBFS	25°C		75.3		dBc
500 MHz	-10 dBFS	25°C		68.1		dBc
1000 MHz	-1 dBFS	25°C		77.0		dBc
1000 MHz	-3 dBFS	25°C		74.5		dBc
1000 MHz	-10 dBFS	25°C		63.0		dBc
TOTAL HARMONIC DISTORTION (THD)						
500 MHz	-1 dBFS	25°C		-76.4		dB
500 MHz	-3 dBFS	25°C		-75.3		dB
500 MHz	-10 dBFS	25°C		-66.2		dB
1000 MHz	-1 dBFS	25°C		-84.5		dB
1000 MHz	-3 dBFS	25°C		-78.2		dB
1000 MHz	-10 dBFS	25°C		-82.0		dB

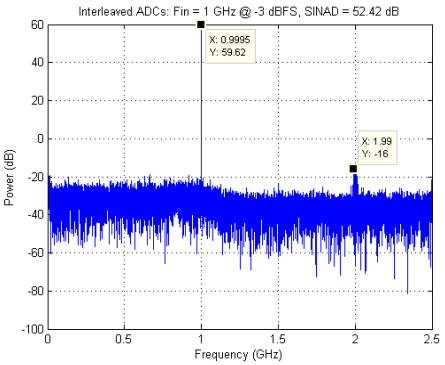
Table 1: FSF-AD15000A Parameters

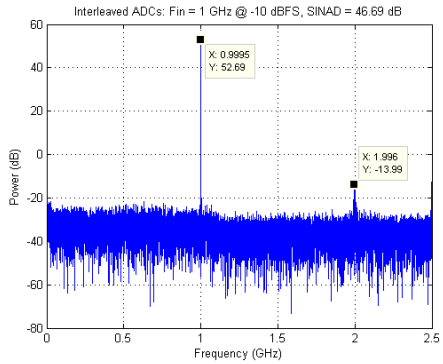












Other sample results

ADC Performance (Fin = 1575 MHz)

Demonstrates that the ADC performance on the FSF-AD15000A is comparable to Analog Devices' published parameters for the individual AD9625-2.5. Also demonstrates that interleaving and interleaving correction does not negatively impact ADC performance.

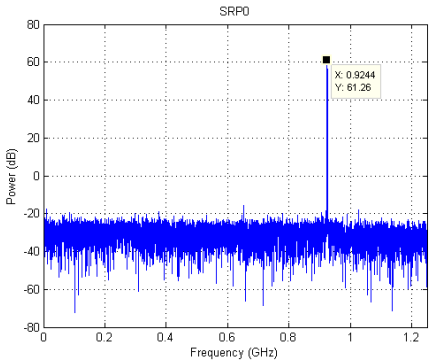
Test conditions

Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

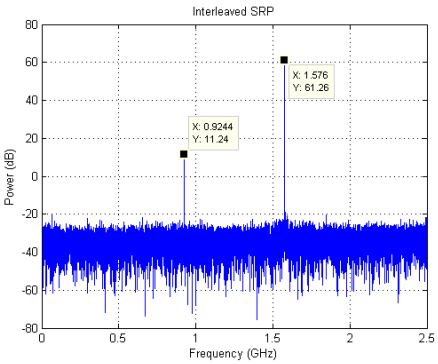
Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
ANALOG INPUT	All tests at Full Scale	25°C				
SIGNAL-TO-NOISE RATIO (SNR)						
1575 MHz	ADI Datasheet Rev. A		54.1	57.0		dBFS
1575 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C		55.7		dBc
1575 MHz	Inter.=ON, Correction=OFF	25°C		48.9		dBc
1575 MHz	Inter.=OFF, Correction=ON	25°C		55.8		dBc
1575 MHz	Inter.=OFF, Correction=ON	25°C		55.7		dBc
SPURIOUS FREE DYNAMIC RANGE (SFDR)						
1575 MHz	ADI Datasheet Rev. A		70	77		dBc
1575 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C		73.5		dBc
1575 MHz	Inter.=ON, Correction=OFF	25°C		50.0		dBc
1575 MHz	Inter.=OFF, Correction=ON	25°C		77.6		dBc
1575 MHz	Inter.=OFF, Correction=ON	25°C		77.1		dBc
EFFECTIVE NUMBER OF BITS (ENOB)						
1575 MHz	ADI Datasheet Rev. A					
1575 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C		70.5		Bits
1575 MHz	Inter.=ON, Correction=OFF	25°C		40.2		Bits
1575 MHz	Inter.=OFF, Correction=ON	25°C				Bits
1575 MHz	Inter.=OFF, Correction=ON	25°C				Bits

Table 2: FSF-AD15000A ADC Performance Assessment at 1575 MHz

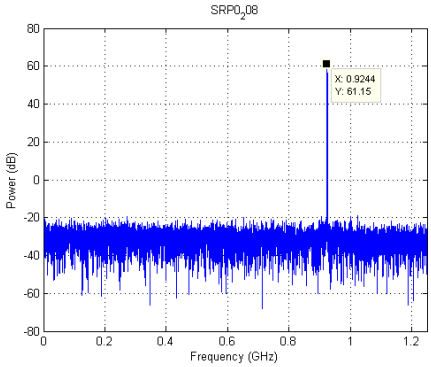
Interleaving=OFF
Interleaving Correction=OFF



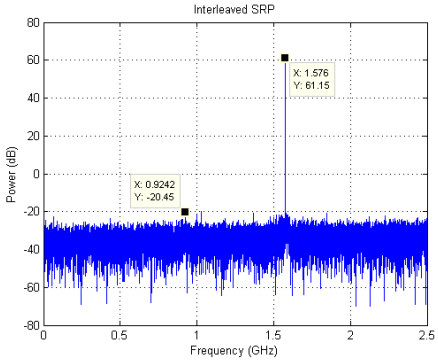
Interleaving=ON
Interleaving Correction=OFF



Interleaving=OFF
Interleaving Correction=ON



Interleaving=ON
Interleaving Correction=ON



ADC Performance (Fin = 1800 MHz)

Demonstrates that the ADC performance on the FSF-AD15000A is comparable to Analog Devices' published parameters for the individual AD9625-2.5. Also demonstrates that interleaving and interleaving correction does not negatively impact ADC performance.

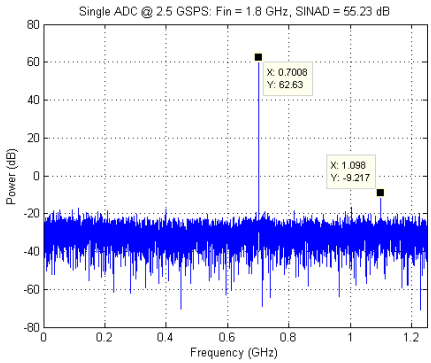
Test conditions

Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

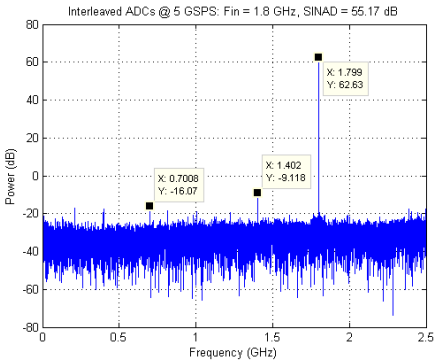
Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
ANALOG INPUT	All tests at -1dBFS	25°C				
SIGNAL-TO-NOISE RATIO (SNR)						
1800 MHz	ADI Datasheet Rev. A					dBFS
1800 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C				dBc
1800 MHz	Inter.=ON, Correction=OFF	25°C				dBc
1800 MHz	Inter.=OFF, Correction=ON	25°C				dBc
1800 MHz	Inter.=OFF, Correction=ON	25°C				dBc
SPURIOUS FREE DYNAMIC RANGE (SFDR)						
1800 MHz	ADI Datasheet Rev. A					dBc
1800 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C				dBc
1800 MHz	Inter.=ON, Correction=OFF	25°C				dBc
1800 MHz	Inter.=OFF, Correction=ON	25°C				dBc
1800 MHz	Inter.=OFF, Correction=ON	25°C				dBc
EFFECTIVE NUMBER OF BITS (ENOB)						
1800 MHz	ADI Datasheet Rev. A					
1800 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C		8.9		Bits
1800 MHz	Inter.=ON, Correction=OFF	25°C		8.87		Bits
1800 MHz	Inter.=OFF, Correction=ON	25°C				Bits
1800 MHz	Inter.=OFF, Correction=ON	25°C				Bits

Table 2: FSF-AD15000A ADC Performance Assessment at 1800 MHz

Interleaving=OFF
Interleaving Correction=OFF



Interleaving=ON
Interleaving Correction=OFF



ADC Performance (Fin = 2750 MHz)

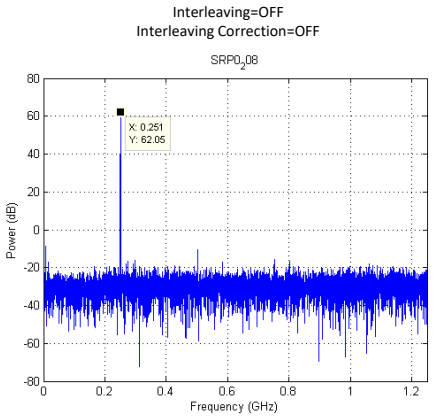
Demonstrates that the ADC performance on the FSF-AD15000A at 2750 MHz.

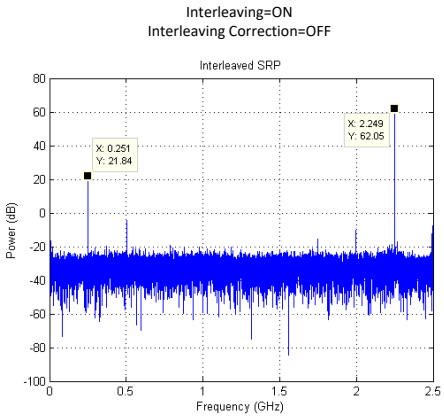
Test conditions

Ambient Temperature: 25 ± 5°C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
ANALOG INPUT	All tests at Full Scale	25°C				
SIGNAL-TO-NOISE RATIO (SNR)						
2750 MHz	ADI Datasheet Rev. A			N/A		
2750 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C		54.1		dBc
2750 MHz	Inter.=ON, Correction=OFF	25°C		40.0		dBc
2750 MHz	Inter.=OFF, Correction=ON	25°C				dBc
2750 MHz	Inter.=OFF, Correction=ON	25°C				dBc
SPURIOUS FREE DYNAMIC RANGE (SFDR)						
2750 MHz	ADI Datasheet Rev. A			N/A		
2750 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C		70.5		dBc
2750 MHz	Inter.=ON, Correction=OFF	25°C		40.2		dBc
2750 MHz	Inter.=OFF, Correction=ON	25°C				dBc
2750 MHz	Inter.=OFF, Correction=ON	25°C				dBc
EFFECTIVE NUMBER OF BITS (ENOB)						
2750 MHz	ADI Datasheet Rev. A			N/A		
2750 MHz	Interleaving=OFF Interleaving Correction=OFF	25°C				Bits
2750 MHz	Inter.=ON, Correction=OFF	25°C				Bits
2750 MHz	Inter.=OFF, Correction=ON	25°C				Bits
2750 MHz	Inter.=OFF, Correction=ON	25°C				Bits

Table 2: FSF-AD15000A ADC Performance Assessment at 2750 MHz





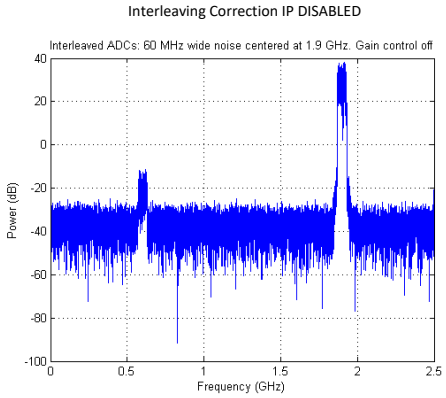
FSF-AD15000A performance w/ wideband noise

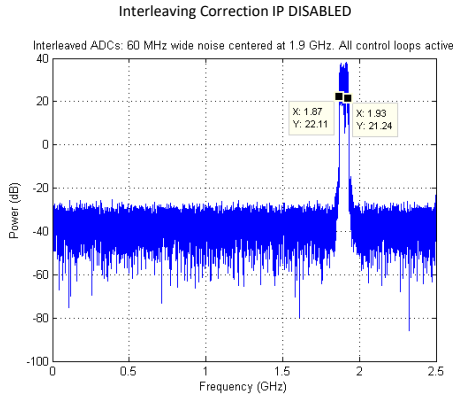
Demonstrates operation of the FSF-AD15000A and interleaving correction IP when challenged with a 60MHz wideband noise source.

Test conditions

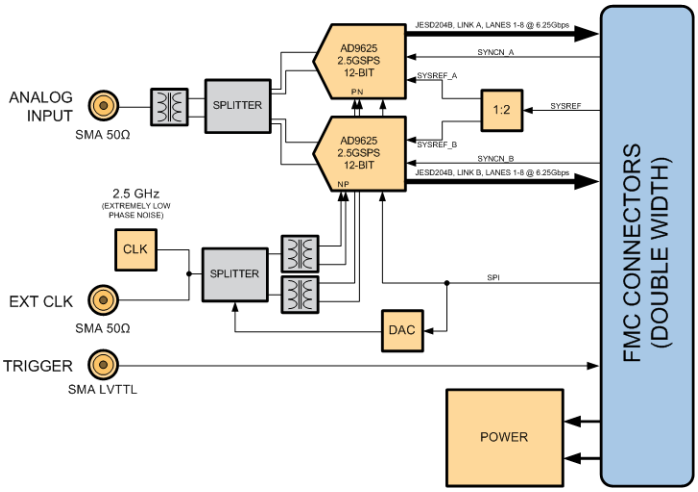
Ambient Temperature: 25 ± 5˚C, Host Platform: Xilinx VC707 Development Kit, RF Signal Generator w/ output filtering, Sample Clock: 2.5 GHz onboard oscillator, Interleaving and Interleaving Correction IP: Dependent on test, Forced Convection (bench top fan), Limited sample size to date

Interleaved ADC; Fin=1900MHz +/- 30MHz (60MHz wideband noise) with and without Interleaving Correction IP Enabled





FSF-AD15000A Block Diagram



Ordering Information

5GSPS, 12-bit ADC JESD204B FMC
PN: FSF-AD15000A
IP core: JESD204B w interleaver
PN: FSI-AD15000A-SRP

Customization Services

Fidus is pleased to offer Hardware, Software, FPGA, Signal Integrity, and Mechanical services related to the integration and customization of this product.

Interfacing and Integration

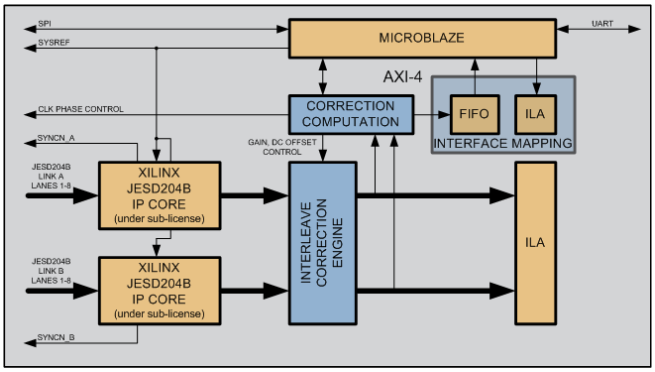
Interface	Description
FMC	
Connector type	HPC (High Pin Count Connector)
Voltage rails	12P0V, 3P3V, 3P3VAUX, VADJ (1.5-3.3V)
JESD204B data i/f	16x MGT data pairs (~6.25 Gbps each)
Analog Inputs	SMA, AC-Coupled, 50Ω, single-ended 0.5 MHz to 3300 MHz, +18 dBm FS
External Clock Input	SMA, AC-Coupled, 50Ω, single-ended 2500 MHz ± 1 MHz, +5 to +15 dBm
Trigger	SMA, DC-Coupled, ~4k to GND
Range	Single ended, (LV)TTL (3.6V max)

Related offerings (additional charges and restrictions may apply)

Part	Description
Native design files	Schematic, Layout, Artwork, Bill of Materials
FPGA code	Demonstration netlist or source code
FPGA IP core	FPGA IP core described below
Application code	Application source code for MicroBlaze®
Customization	Customization to fit individual needs

FPGA IP

Fidus has completed the DSP work required to either reduce or cancel the spectral content that is related to the interleaving process. The following diagram depicts the FSI-AD15000A-SRP core.



Sales and Support

For additional information, questions or request for quotation visit: www.fidus.com

Customize your FS-AD15000A

Speak with our Design Services Group on how to accelerate your custom design: design@fidus.com

About Fidus

Fidus Systems, founded in 2001, specializes in leading-edge electronic product development with offices in Ottawa and Waterloo Ontario, and San Jose, California. Our hardware, software, FPGA and signal integrity teams architect, design and deliver next-generation products for clients in emerging technology markets. We build long-term relationships by consistently exceeding expectations.

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