

## how we Help

Do you want to: Increase your **revenue**? Reduce your **costs**? Increase your **speed** and **flexibility**? Focus on your **core competency**?

Consider Fidus for electronic product development and consulting services.

Signal Integrity (SI), Power Integrity (PI), and EMC are not big and bad and scary, they are just too often misunderstood or neglected. Time-to-market, repeated Regulatory failures, engineering debug, and PCB re-spin costs are the most apparent results of not carefully considering SI, PI and EMC. The hidden expense of not giving SI, PI, and EMC the proper attention is in the product's Bill of Materials and Assembly costs. These unnecessary product costs are attributed to items such as excessive capacitors, ferrite beads, shields, and manually provisioned RF absorbers. The Fidus team helps you avoid these pitfalls.

### Fidus – an excellent choice

At Fidus Systems, we understand the unique challenges faced by technology companies – too many projects and too few engineering resources. With top engineering talent, multiple design centers and on-site staffing options, Fidus provides highly responsive engineering teams that are an extension of your development team to successfully bring products to market faster.

Recognized as a trusted design partner, Fidus is dedicated to meeting customer expectations, and developing long-term relationships with clients built on integrity, quality and open communications.

Fidus is pleased to provide customers with full end-to-end development solutions or more selective targeted engagements.

Fidus has delivered more than 1500 projects for 300+ clients, from Tier-1 multinationals to SMEs to start-ups. Fidus is headquartered in Ottawa, Canada with local design centers in Kitchener-Waterloo and San Jose.

## design Expertise

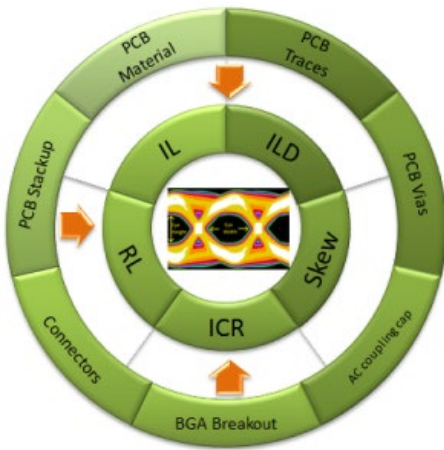
- Fidus delivers SI, PI, and EMC analysis for on-chip IC design, package design, PCB-level, and system design.
- Layer stack-up, hybrid technologies, via, and net topology design
- Capabilities and experience to 40GHz+ and 25Gbps+
- IBIS model simulations, including Power Aware IBIS v5.0
- Pre-layout, during layout, and post-route, high-speed signal integrity analysis and simulation for verifying signal quality, reducing signal reflections, increasing timing margins, reducing crosstalk, enhancing power integrity through cost effective decoupling design, simultaneous switching noise (SSN) reduction and reducing conducted and radiated emissions
- Expertise in high-speed memory interfaces (DDR3 and DDR4)
- Specific Absorption Rate (SAR) analysis
- Component & system characterization, measured or simulated including full S-parameters, gain & noise figure optimization
- Shield designs for both compliance and sensitive signal preservation

## tools for High-end development

- **Fidus maintains licenses for:** Agilent® ADS, ANSYS® HFSS™, Cadence® Sigrity SI/PI Solution, Mentor Graphics® HyperLynx®, Cadence PSpice®, Synopsys® HSPICE®
- **RF laboratory equipment:** Agilent® Network Analyzer, Agilent Vector RF/Signal Generator, Agilent PXA Signal Analyzer, Agilent Digital Signal Analyzer, HP® Signal Generators, Agilent Electronic Loads, Spectrum Analyzers, multi-channel oscilloscopes to 40 GS/s



ALLIANCE PROGRAM  
PREMIER MEMBER



### bringing you Xilinx premier

As Xilinx Premier, Fidus receives exclusive training, certification, and early-access to tools, IP, and new silicon. By invitation, Fidus was *the* inaugural Xilinx Premier Design Services member in North America. This means that when you hire Fidus, you know that Fidus is on the forefront of Xilinx's roadmap, experienced in the most advanced tool flows, and is top of mind within the Xilinx support network.

### Locations

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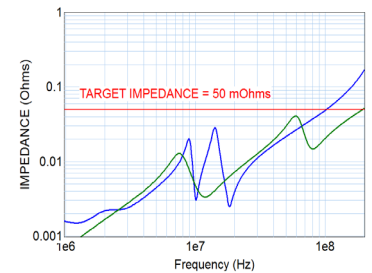
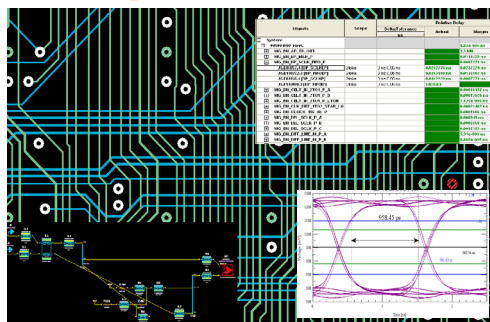
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### Examples of our work



#### High-speed memory interfaces

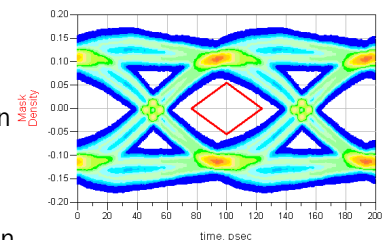
- DDR2, DDR3, DDR4 memories and modules
- Cross talk reduction
- Topology templates and routing guidelines
- Pre- and post-route simulation
- Dynamic timing verification

#### Power Integrity

- Design for target impedance
- Optimize PCB stackup for power distribution
- Optimize number and location of decoupling capacitors
- SSO noise reduction

#### SerDes design and optimization

- Experience with 56Gbps PAM4 designs
- Link budgets
- Interconnect optimization
- Pad compensation
- s-parameter and eye diagram simulation
- Pre-emphasis and equalization



#### System design

- Power, grounding, decoupling and filterin
- 28Gbps SFP+ and QSFP+ Cable adapter modules
- High-speed backplanes
- Multi-gigabit serial links
- 3D heat sink and enclosure modeling for EMI

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