FSF-AD8200A

8-Channel, 185MSPS JESD204B ADC FMC

2015

Features

- Transformer-coupled 14-bit, 185 MSPS ADC on each of 8 channels in HPC FMC form-factor
- JESD204B Subclass 1 feature set including deterministic latency
- Designed for compatibility with ANSI/VITA 57.1
- Analog input bandwidth: 4.5MHz – 500MHz (-3dB)
- Ch-to-ch crosstalk below –75dB @ 183MHz
- High performance on-board clock generator capable of sub-100fs jitter
- External clock and trigger inputs
- Designed for experimentation, development, and integration into end systems
- 0 to +45°C operating temperature range (with heat sink , natural convection)
- Full-scale input range programmable between 1Vpp and 2Vpp in 1dB steps
- Xilinx® VC707 .bit file demonstration design
- Designed for compatibility with Xilinx® ML605 (2x 4ch), KC705 (4-ch), VC707, and VC709. Operation demonstrated on VC707.
- ADC Multiple Device Synchronization (MDS) for coherent sampling across all ADC channels (JESD204B class MCDA-ML)
- Powered entirely through the FMC connector

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8-Channel, 185MSPS JESD204B ADC FMC

The FSF-AD8200A is an 8-channel analog-to-digital conversion board based on four IDT® ADC1443D dual-channel, 14-bit, 185MSPS ADCs.

The FSF-AD8200A targets evaluation, development, experimentation, and system integration applications. The JESD204B feature of the FSF-AD8200A enables multi-channel coherent waveform digitization. Examples of systems that may benefit from the capabilities of the FSF-AD8200A include general experimentation/instrumentation, SDR, MIMO antenna, ultrasound, AESA radar, and spectrum sampling.

Description

The FSF-AD8200A is an 8-channel analog-to-digital converter FMC, designed to be electrically and mechanically compatible with the ANSI/VITA 57.1 specification. Designed with four IDT ADC1443D dual 14-bit, 185 MSPS converters; this solution offers instrumentation, communications, defense, and aerospace equipment development engineers easy access to broadband, coherent multi-channel data acquisition applications using the latest JESD204B interface standard.

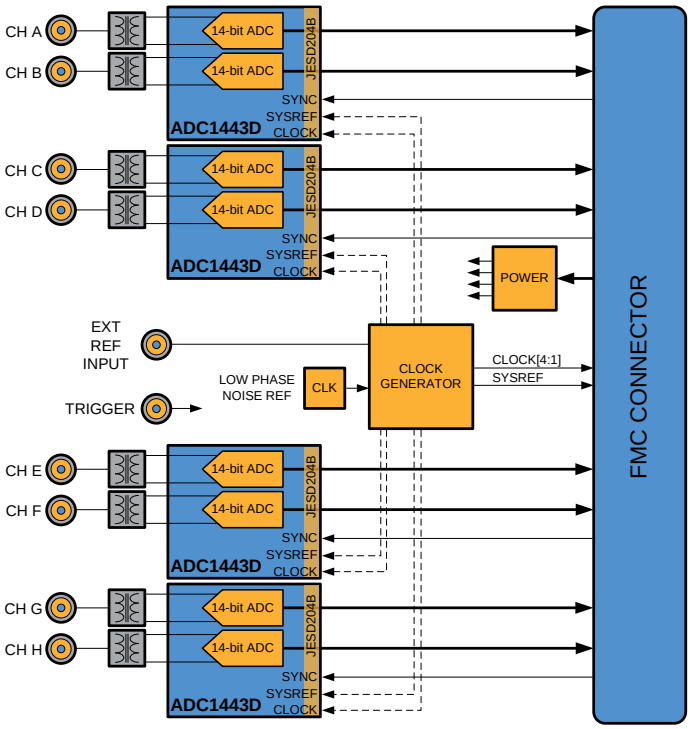
The deterministic latency feature specified within JESD204B helps to ensure that the downstream post-processing device is being presented with 8-channels of synchronized data across system power cycles and resets. At the physical layer- once sampled- the data from each ADC channel is transmitted on a high-speed serial bus to the downstream device. This serial data architecture minimizes downstream I/O pin count and increases performance by lowering system noise. Similarly, PCB layer count requirements are relaxed compared to a parallel or multi-lane LVDS data bus design.

Extra care has been incorporated in the design of the FSF-AD8200A to ensure extremely low jitter on the ADC sampling clocks. Low jitter performance is critical in preserving the full dynamic range of the converters when high frequency analog inputs are exposed to both wanted and unwanted wide dynamic range signals. In addition, careful layout and shielding ensures excellent channel-to-channel isolation.

The FSF-AD8200A is an ideal starting point for broadband, high fidelity waveform digitization experimentation. It is also a great platform to get up and running quickly with a JESD204B interface. Finally, it serves as an easy drop-in solution for end-systems that require a multi-channel, synchronized waveform digitizer.

Applications

- General experimentation and instrumentation
- ADC1443D test and qualification
- Various software defined radio (SDR) implementations
- MIMO antenna subsystems
- AESA radar systems
- RF direct-conversion front-ends



FSF-AD8200A block diagram

About Fidus

"FMCs by Fidus" is a brand of Fidus Systems Inc. Fidus provides clients with greater flexibility and capability in their product development through access to the expertise, processes and tools to transform their concepts to products. Fidus has delivered on more than 1000 products and projects for approximately 300 customers across North America.

For more information, visit www.fidus.com.

Ordering Information

8-Channel ADC JESD204B FMC PN: FSF-AD8200A
10-pack, 12" SSMC-to-SMA cables PN: FSA-SSMC2SMA

Contact

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Typical Performance

Parameter	Typical	Unit
3dB Bandwidth	4.5 to >500	MHz
Fin = 4.989MHz		
SNR	69	dBc
SFDR	83.2	dBc
THD	-79	dBc
Coupling (adjacent)	-88.2	dB
Coupling (2nd adjacent)	-100.3	dB
Fin = 183.561MHz		
SNR	61.7	dBc
SFDR	70.2	dBc
THD	-74.8	dBc
Coupling (adjacent)	-77.5	dB
Coupling (2nd adjacent)	-100.4	dB

Test conditions:
Temperature: 25 ± 5°C
Test Platform: Xilinx VC707 development kit
Sample Rate: (178 + 4/7) MSPS

Interfaces

Interface	Description
FMC Connector	
Connector type	HPC (High Pin Count Connector)
Voltage rails	12P0V, 3P3V, 3P3VAUX, VADJ (1.5-3.3V)
JESD204B data i/f	8x MGT data pairs (~3.7Gbps each)
Analog Inputs	SSMC, AC-Coupled, 50Ω, single-ended
External Clock Input	SSMC, AC-Coupled, 50Ω, single-ended
Trigger	SSMC, DC-Coupled, ~4k to GND
Range	Single ended, (LV)TTL (5V tolerant)

Support information

- User manual
- Quick start guide
- Command interpreter guide
- Demonstration .bit file for Xilinx® VC707 development kit
- Schematics (upon request)

Related offerings (additional charges and restrictions may apply)

Part	Description
Cables	10-pack, 12" long SSMC-to-SMA adapter cables
Schematic	Native schematic file
PCB Layout	Native layout file
FPGA code	Demonstration netlist or source code
Application code	Application source code for MicroBlaze®
Customization	Customization to fit individual needs

FSF-AD8200A with heat sink

The custom designed heat sink helps to ensure thermal margins in conduction cooled environments up to 45°C.

Customization Services

Fidus is pleased to offer Hardware, Software, FPGA, Signal Integrity, and Mechanical services related to the integration and customization of this product. Please refer to the *Contact* section of this datasheet.